In re Appln. of ISHIDA et al.
Application No. 09/877,037

REMARKS

In response to the Examiner's Action mailed October 23, 2002, Applicants request reconsideration in view of the following remarks. No claims are added or cancelled so that claims 13-16 remain pending.

An Information Disclosure Statement is being filed simultaneously with this Response. An indication of consideration of the publications in the next communication is respectfully requested.

In response to the Examiner's request it is proposed to add a "prior art" legend to Figures 10(A), 10(B), and 11.

There has been no prior art rejection and the sole basis of rejection is 35 USC 112, first paragraph. The Examiner renewed the assertion that the claims are not enabled by the disclosure. Some of the remarks of the previous Official Action were carried over but obviously do not apply. For example, the Examiner stated that the "applicant fails to disclose the type of capacitor". This statement is incorrect as to the claims now pending. As mentioned in the following sentences in the Official Action, the capacitor is an MIM capacitor.

Further, the Examiner asserted that the "applicant fails to disclose how the MIM capacitor is changeable inversely with the thickness of the insulating film." The Applicants do not have to state that information because it is so well known in the art and in the fundamental physics of capacitors that no description is necessary. The disclosure of a patent application is directed to one of skill in the art. Thus, fundamental scientific principles do not have to be explained.

To demonstrate that knowledge in the art, attached are pages 41-47 of "MMIC Design GaAs FETs and HEMTs", Ladbrooke (1989). These pages discuss capacitors commonly used in MMIC's, including MIM capacitors. The discussion concerning MIM capacitors is particularly found on pages 45-47 and attention is directed to equation (3.12) on page 45. It is apparent from that fundamental equation, which is taught in every first year college physics course, that the capacitance of an MIM capacitor varies inversely with the thickness of the dielectric film between the two plates of the capacitor.

Of course, the other part of the invention involves the parasitic capacitance with regard to the transistor that is part of the claimed structure. As also well known to those of skill in the art, in manufacturing MMIC's, a dielectric film that is deposited to form an MIM capacitor is also deposited on the MMIC substrate and produces a parasitic capacitance with respect to transistors on the substrate. That knowledge in the art is demonstrated by two attached prior art publications.

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First, attached is an excerpt from a Japanese language publication "Microwave Semiconductor Circuits-Basis and Application" (1993). The typical structure of an MMIC is shown in Figure 5.16 of that publication and an additional enlarged copy of that drawing with English language titles is attached to the publication. As can be seen from that figure, just as described in the patent application at pages 2 and 3, a capacitor and a transistor, in the case of the figure an HEMT, are formed on the same substrate with a result that excess parts of the insulating film deposited in formation of the MIM capacitor are unavoidably disposed around the transistor. This excess insulating film produces a parasitic capacitance that increases in capacitance with increasing thickness of the insulating film. (See the present patent application from page 2, line 31 through page 3, line 7)

In further substantiation of the increase in parasitic capacitance with the thickness of an insulating film in an MMIC, attached are pages 62-65, 281-284, and 290-297 of "Modern GaAs Processing Methods" Williams (1990). Attention particularly is directed to the paragraph beginning on page 281 and ending on page 282 describing the parasitic capacitance and its increase with thickness of the insulating film. Pages 62-65 provide an explanation of a model of a transistor in an MMIC and its parasitic capacitance. Further, although discussed in Ladbrooke, cited above, pages 293-294 of Williams also describe MIM capacitors and their increase in capacitance with a decrease in the thickness of the dielectric film of those capacitors.

The invention as defined in the independent claims includes a transistor and an MIM capacitor connected to the transistor. An insulating film is disposed around the transistor and, as explained and understood in the art, that insulating film alters the input and output capacitances of the transistor because of the parasitic capacitance. As already described, known in the art, and shown in the attached publications, those input and output capacitances vary directly, i.e., in the same direction, with the thickness of the insulating film. The parasitic capacitance increases as the film thickness increases. This variation is directly opposite to the change in capacitance of an MIM capacitor when the dielectric film between the plates of that capacitor changes in thickness as shown in the attached publications. The capacitance of the MIM capacitor decreases as the thickness of the insulating film increases, as supported by the attached publication excerpts.

In the invention, these opposite direction changes in the two capacitances with the change in thickness of the insulating film is advantageously exploited. In all claims, the capacitor includes two metal electrodes that are separated by that insulating film. Thus, that capacitor has a capacitance that changes inversely with the thickness of the insulating film. One of those metal electrodes is connected to an input terminal of the transistor in the structure of claim 13 and to the output terminal of the transistor in the structure of claim 15.

Therefore, in a fabrication process for the claimed MMIC, when the thickness of the insulating film varies from a design value, causing a change in the capacitance of the capacitor and of the input and output capacitances of the transistor, by using that insulating film as the dielectric film of the MMIC, the changes in transistor's capacitances and in the capacitance of the capacitor tend to compensate each other and, ideally, cancel each other. Thus, the desired performance of the MMIC is obtained even when variations in process conditions occur that cause variations in the thickness of the insulating film.

As pointed out in the previous response, this effect, which is the result of the claimed structure, is clearly disclosed in the patent application at numerous locations including pages 8-10, 12, and 13. One of skill in the art fully understands what is claimed, namely a transistor and a capacitor with the dielectric of the capacitor being part of an insulating film that surrounds the transistor, and with one plate of the capacitor connected to a terminal of the transistor. That person of skill in the art would readily comprehend the advantageous effect of the invention, namely improved tolerance of process condition variations, and how that effect is achieved. Therefore, the claimed invention is enabled by the disclosure.

Upon reconsideration, the rejection of the claims as not enabled should be withdrawn and the claims should be examined on the merits, i.e., in view of the prior art.

Respectfully submitted,

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